PATENT APPLICATION TRANSMITTAL LETTER (Large Entity)	Docket No. MICT-0042-US (99-0220)

TO THE ASSISTANT COMMISSIONER FOR PATENTS

Transmitted herewith for filing under 35 U.S.C. 111 and 37 C.F.R. 1.53 is the patent application of:

CHANDRA V. MOULI

For: **FORMING SIDEWALL OXIDE LAYERS FOR TRENCH ISOLATION**

Enclosed are:

- ☒ Certificate of Mailing with Express Mail Mailing Label No. **EL218153166US**
- ☒ **Two (2)** sheets of drawings.
- ☐ A certified copy of a application.
- ☒ Declaration ☒ Signed. ☐ Unsigned.
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For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	45	- 20 =	25	x	$18.00	$450.00
Indep. Claims	6	- 3 =	3	x	$78.00	$234.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$760.00
					TOTAL FILING FEE	$1,444.00

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Dated: **August 23, 1999**

Signature

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MICT-0042-US
(99-0220)

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: FORMING SIDEWALL OXIDE LAYERS FOR TRENCH ISOLATION

INVENTOR: CHANDRA V. MOULI

Express Mail No.: EL218153166US

Date: August 23, 1999

FORMING SIDEWALL OXIDE LAYERS FOR TRENCH ISOLATION

Background

This invention relates generally to forming shallow trench isolation structures in making semiconductor devices.

Particularly in advanced processes, shallow trench isolation (STI) has significant advantages over local oxidation of silicon (LOCOS) in terms of scalability. Compared to LOCOS, STI reduces oxide encroachment into the active area and hence facilitates achieving compact cell designs. However, the STI process is known to increase leakage currents which affect performance. One application of STI processes is making dynamic random access memory (DRAM) devices.

The stress created in the top and bottom corners of the trench sidewall used in STI processes is one source of leakage current. The STI process usually involves an anisotrophic etch into the silicon surface. A sidewall oxidation step grows oxide on the sidewalls of the trench. The trench sidewall contains several possible crystallographic orientations and the interface trap density is higher in the sidewall than on the silicon surface. The sidewall oxide is designed to smooth this interface and to reduce the stress in the silicon.

The oxidation rate in stressed silicon is low. Thus, the thickness of the sidewall oxide at the corner between the silicon surface and trench may be reduced. To overcome this problem, oxidation is done at a high temperature to increase the oxide thickness. However, increasing the thermal budget is generally undesirable. For example, increasing the temperature increases the depth of all the existing junctions. In advanced semiconductor processes with extremely small geometries, this is a disadvantage.

One potential solution to the problem of thin sidewall oxides at the corner between the upper surface and the trench is to create crystallographic damage at this point. It is known that such damage increases the oxidation rate. Therefore, by creating a highly damaged region at the corner, the thickness of the sidewall oxide may increase.

However, creating damage in the silicon substrate at exactly the position where stresses are known to occur may be counterproductive. In fact, the net effect of creating such damage may be to increase the possibility of leakage currents. The implant damage creates a compressive stress. As a result, crystallographic defects may create leakage causing interface states. The generation and recombination centers increase as a result of increased crystallographic defects. The use of high energy implants to create damage creates nucleation sites which create defects which may also result in increased leakage currents.

Thus, there is a continuing need for a way of producing high quality sidewall oxides without unnecessarily creating silicon damage that may result in increased leakage currents.

Summary

In accordance with one aspect of the present invention, a method of forming a trench isolation includes injecting impurities into a region in the semiconductor structure. A trench is made through the impurity laden region leaving a portion of the impurity laden region around the trench.

Other aspects are set forth in the accompanying detailed description and claims.

Brief Description of the Drawings

Figs. 1-6 are greatly enlarged, partial cross-sectional views showing steps used in one embodiment of the present; and

Fig. 7 is greatly enlarged, partial cross-sectional view in accordance with another embodiment of the present invention.

Detailed Description

Referring to Fig. 1, a conventional semiconductor layer 10 may be used as the semiconductor structure for forming integrated circuit devices with shallow trench isolation (STI). For example, the layer 10 may be bulk

silicon or it may be an epitaxial layer formed over a bulk silicon layer. A dielectric layer 12, commonly called a pad oxide, may be formed over the structure 10. The layer 12 may be formed using any conventional technique including thermal oxidation or deposition. For example, the layer 12 may be formed by chemical vapor deposition (CVD) or by the decomposition of tetraethyl orthosilicate (TEOS). In accordance with conventional silicon trench isolation processes, a nitride layer 14 may be formed over the layer 12. Conventionally, the nitride layer 14 is formed by chemical vapor deposition.

An anti-reflective coating 16 may be patterned on top of the nitride layer 14. The anti-reflective coating 16 may be used in advanced lithographic processes to define a pattern for etching through the layers 12 and 14. However, other patterned mask layers may be used, such as those using photoresist.

Referring next to Fig. 2, an anisotropic etching process may be used to form an opening 18 through the nitride layer 14 and the dielectric layer 12 down to the surface of the layer 10. Thereafter, the surface of the layer 10 may be cleaned if desired.

Next, a solid diffusion source 20 may be deposited into the opening 18. Suitable solid diffusion sources include borophosphosilicate glass (BPSG) materials doped with an oxidation enhancing species such as argon, or other

inert species or oxygen. The source 20 allows impurities in the source to diffuse into the layer 10 when exposed to modest temperatures. As a result of the diffusion, the impurities form a diffused region 22 defined by the masking action of the opening 18. A typical solid source diffusion step may involve 800°C for about twenty minutes.

Through the use of a solid diffusion source, an impurity laden region 22 containing oxidation enhancing impurities may be formed in the layer 10. The region 22 need not unnecessarily create interface states, generation and recombination centers, or other damage effects which may adversely effect the performance of the resulting STI.

As illustrated in Fig. 4, an anisotropic etch forms a trench 24, which may have substantially vertical sidewalls 25. The anisotrophic etch is masked by the layers 12 and 14, which also act as the mask for the solid source diffusion. Thus, the trench 24 extends through the oxidation enhancing impurity region 22 leaving the portion 22a around the trench 24. The portion 22a corresponds to the underdiffusion which necessarily results in the course of the solid source diffusion process illustrated in Fig. 3.

The amount of underdiffusion and thus the lateral and vertical extent of the region 22a is a function of the concentration of impurities in the source 20 and the time and temperature of the diffusion step. As a result of the

fact that the same mask is used for the etch and the diffusion, the region 22a is situated precisely at the corner 23 between the upper surface of the structure 10 and the trench 24. This is precisely the region which may be prone to thin oxide thicknesses, which, in turn, may give rise to leakage currents.

Turning next to Fig. 5, a sidewall oxidation process forms the sidewall oxide 26. Because of the oxidation enhancing affect of the impurities in the region 22a, the thickness of the sidewall oxide 26 at the corner is increased and the corners 23a are substantially rounded as a result of the oxidation process, improving the performance of the sidewall oxide 26.

Finally, referring to Fig. 6, a trench filler material 28, such as a deposited oxide, may fill the trench lined by the sidewall oxide 26. By using high pressure deposition techniques, the trench 24 may be readily filled despite the fact that the trench 24 has relatively vertical sidewalls 25. By making the sidewalls 25 relatively vertical, the possibility of etching away the region 22a during the trench etching step is reduced.

An alternate embodiment of the present invention, shown in Fig. 7, uses ion implantation to form the region 32a which corresponds to the region 22a in the embodiment of Fig. 4. After the step illustrated in Fig. 2, the resulting structure is exposed to an ion implantation 30.

The implant species is preferably a species which enhances oxidation. Suitable species include argon, other inert elements and oxygen. Inert species are desirable because they do not contribute carriers to the semiconductor structure.

The implant acts to enhance oxidation rather than to create crystallographic damage which could cause leakage currents. As a result of lateral straggle, a portion 32a of the implanted region extends under the masking layers 12 and 14. The extent of lateral straggle (species movement transverse to the implant direction) is a function of the dose and implant energy. Generally, about 20 percent of implanted species are subject to lateral straggle.

In some embodiments of the present invention, it may be desirable to use an angled implant to produce the region 32a. By using an angled implant and rotating the layer 10, additional impurities may be caused to enter the region 32a. Of course, it should be understood that the height of the structure produced by the layers 12 and 14 is substantially less than what is depicted in the enlarged drawing of Fig. 7 and therefore the effect of the angled implant may be more substantial than it would appear from Fig. 7. Implant angles as high as 30° may be used in some embodiments. However, even where an angled implant is used, since the regions 32a are shielded below an implant mask they are primarily formed by lateral straggling.

To minimize the amount of crystallographic damage that results from the implant, it is desirable to use a relatively low energy implantation. For example, implantation energies of less than 20 keV are generally desirable and in some embodiments implantation energies of less than 10 keV may be used.

It is known that argon has an effect in enhancing oxidation which is not the result of damage to the silicon substrate. See Semiconductor International, Vol. 22, No. 2, February 1999. It is believed, without limiting the present invention, that the presence of argon makes it easier for oxygen to form oxygen-to-silicon bonds. It is believed that this is due to the fact that the silicon to silicon bond energy is higher than the argon to silicon bond energy so that the argon is more easily replaced if the argon is positioned substitutionally within the lattice. With interstitial argon species, the wave functions of silicon and argon are believed to interact to relax the bond strength.

Again, without limiting the present invention, it is believed that oxygen implants may similarly improve oxidation in a way which is not dependant on crystallographic damage effects. Oxidation is limited by the diffusion of oxygen into silicon and the diffusion of oxygen through any overlying oxidation layers. By implanting the oxygen under the surface of the silicon, it

is believed that oxidation may be enhanced by the presence of the oxygen in the silicon structure, separate and apart from any damage created by the implant.

While a passivation layer may be utilized over the semiconductor layer 10 for the implantation, it may be advantageous in some embodiments to dispense with a passivation layer. This is because the use of a passivation layer may necessitate higher implant energies.

Because of the low implant energies that may be used, high doses may be used in some embodiments. For example, argon may be implanted at doses of approximately 1×10^{15} atoms per square centimeter. In some embodiments, it may desirable to use a relatively low temperature, short duration heat step to repair any damage which may result from the low energy implants. It is not believed that it is necessary for the argon species to be substitutional to have the oxidation enhancing effect.

After the implanted region 32 has been formed, the ensuing process steps follow the steps illustrated in Figs. 4-6 and described previously. Namely, a trench 24 is formed through the implanted region 32 leaving the regions 32a, formed at least in part by lateral straggle, to either side of the trench. Thereafter, a sidewall oxide 26 is formed creating the round corners 23a. Finally, as shown in Fig. 6, the trench is filled with the trench filler material 28.

Thus, in accordance with embodiments of the present invention, an oxidation enhancing material may be positioned precisely at the corner where reduced oxidation normally occurs. As a result, in some embodiments, oxidation may be enhanced without significantly increasing the thermal budget for the process. In some embodiments, oxidation may be enhanced while actually reducing the thermal budget by reducing the temperatures or the times of high temperature steps commonly used in the sidewall oxidation step to overcome the reduced oxidation at the corner. At the same time, it is possible to decrease the disruption of the crystallographic structure at the corner region which would otherwise give rise to the possibility of crystallographic damage, interface states, generation and recombination centers and other defects which may produce leakage currents.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. A method of forming a trench isolation comprising:

forming a region containing oxidation enhancing impurities in a semiconductor structure; and

making a trench through said region, leaving a portion of said region around said trench.

2. The method of claim 1 wherein forming said region includes forming said region using ion implantation.

3. The method of claim 2 wherein using ion implantation includes using implantation at energies below 20 keV.

4. The method of claim 1 wherein forming said regions includes implanting impurities which enhance the oxidation of said structure beyond that which would be expected from crystallographic damage effects.

5. The method of claim 4 further including implanting argon.

6. The method of claim 4 further including implanting oxygen.

7. The method of claim 3 wherein using implantation further includes using an angled ion implant.

8. The method of claim 1 wherein making a trench includes forming a trench by an anisotropic etch to create substantially vertical sidewalls.

9. The method of claim 1 wherein forming a region includes causing diffusion to occur from a solid diffusion source.

10. The method of claim 1 including forming said region before making a trench.

11. The method of claim 1 including using the same mask to form the region and the trench.

12. A method of forming a trench isolation comprising:

forming a trench in a semiconductor structure; and

implanting an oxidation enhancing species in a region proximate to the trench using an implant energy of less than about 20 keV.

13. The method of claim 12 wherein implanting includes implanting at an energy of less than 10 keV.

14. The method of claim 12 including implanting inert species.

15. The method of claim 14 including implanting argon.

16. The method of claim 12 including implanting oxygen.

17. The method of claim 12 wherein implanting includes implanting said species at an angle.

18. The method of claim 12 including implanting before forming a trench.

19. The method of claim 12 including using the same mask for implanting and forming a trench.

20. A method of forming a trench isolation comprising:

depositing a solid source diffusion layer on a semiconductor structure;

causing impurities from said diffusion layer to diffuse from said layer into said structure; and

forming a trench through said impurities in said structure.

21. The method of claim 20 wherein depositing a solid source diffusion layer includes depositing a doped glass layer.

22. The method of claim 20 wherein depositing a solid source diffusion layer includes depositing a layer doped with argon.

23. The method of claim 20 further including forming a masking layer, defining an opening in said masking layer, and depositing said diffusion layer into said opening.

24. The method of claim 23 including using said masking layer to form said trench.

25. The method of claim 23 wherein forming said masking layer includes forming a pad oxide covered by a nitride layer.

26. A method of forming a trench isolation comprising:

forming a trench into a semiconductor material and defining an edge at the surface of said semiconductor material; and

forming a region, proximate said edge, formed primarily of laterally scattered impurities.

27. The method of claim 26 wherein forming a region includes using ion implantation to form an implanted region with lateral scattering and thereafter forming said trench by etching through said implanted region.

28. The method of claim 26 wherein forming an region includes implanting argon.

29. The method of claim 28 wherein forming a region includes defining an opening in a masking layer including a nitride layer over an oxide layer.

30. The method of claim 26 wherein forming a region includes ion implanting oxidation enhancing impurities at energies of less than about 20 keV.

31. The method of claim 26 further including forming a thermal sidewall oxidation layer on said trench.

32. The method of claim 26 wherein forming a region includes ion implanting an inert species.

33. A method of forming a trench isolation comprising:

defining an opening in a masking layer over a semiconductor structure;

causing impurities to enter a portion of said structure through said opening; and

using said mask to form a trench through the portion of said structure containing said impurities.

34. The method of claim 33 wherein defining an opening includes forming a pad oxide covered by a nitride layer.

35. The method of claim 33 wherein causing impurities to enter said semiconductor structure includes ion implanting said impurities.

36. The method of claim 35 including implanting inert impurities.

37. The method of claim 36 including implanting argon.

38. The method of claim 35 including implanting oxygen.

39. The method of claim 35 including ion implanting at energies of less than 20 keV.

40. The method of claim 33 wherein causing impurities to enter a portion of said semiconductor structure includes depositing a solid diffusion source over said masking layer and diffusing impurities from said source into said structure through said opening.

41. The method of claim 33 including causing impurities to enter said structure, which impurities enhance oxidation separate and apart from any crystallographic damage effects.

42. A semiconductor integrated circuit device formed by a process comprising:

forming a region containing oxidation enhancing impurities in a semiconductor structure; and

making a trench through said region, leaving portions of said region on both sides of said trench.

43. The device of claim 42 formed by a process further comprising ion implanting said oxidation enhancing impurities.

44. The device of claim 42 formed by a process further comprising ion implanting argon to form said region.

45. The device of claim 42 formed by a process further comprising forming a region containing oxidation enhancing impurities by diffusing those impurities from a solid diffusion source.

FORMING SIDEWALL OXIDE LAYERS FOR TRENCH ISOLATION

Abstract of the Disclosure

A shallow trench isolated integrated circuit may be formed by creating an oxidation enhancing region at the corner between a semiconductor structure surface and the trench. This region may be formed by ion implantation or solid source diffusion in a way which decreases crystallographic defects. As a result, oxidation at the trench may be enhanced without adverse effects on leakage currents. In some embodiments, the impurity laden region is formed first and the trench is etched through the region leaving an impurity laden remnant at the corner between the trench and the structure surface.

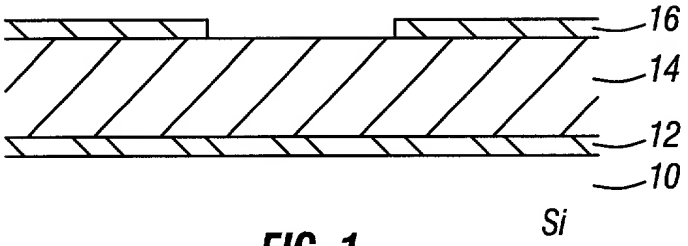

FIG. 1

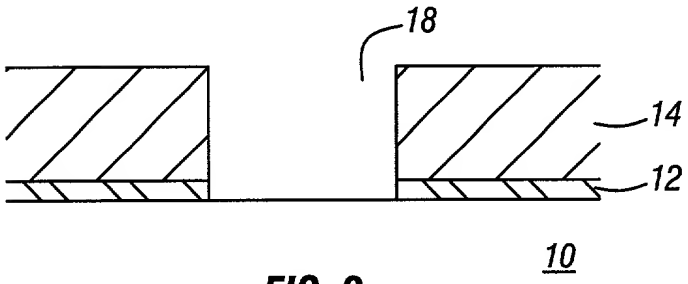

FIG. 2

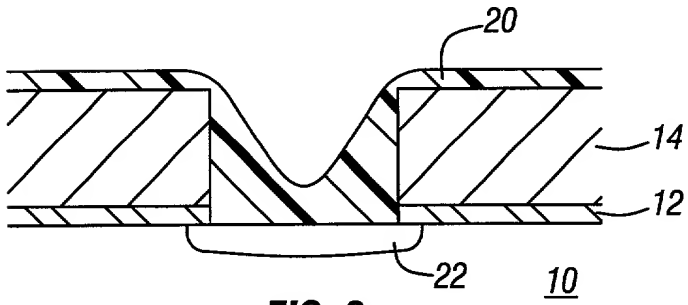

FIG. 3

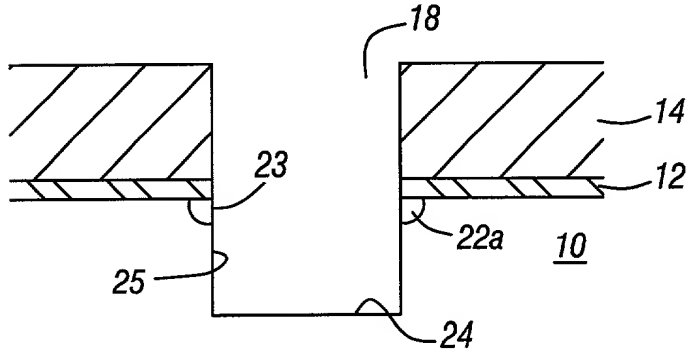

FIG. 4

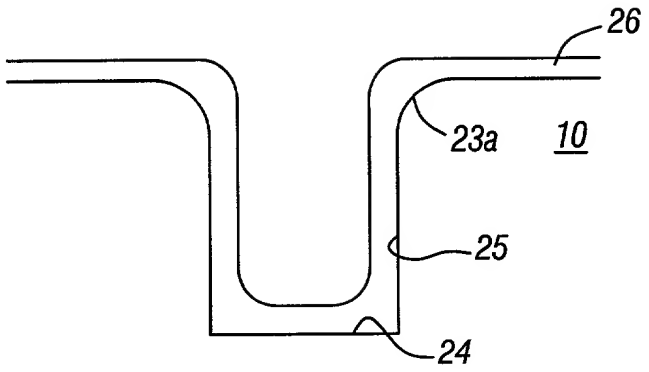

FIG. 5

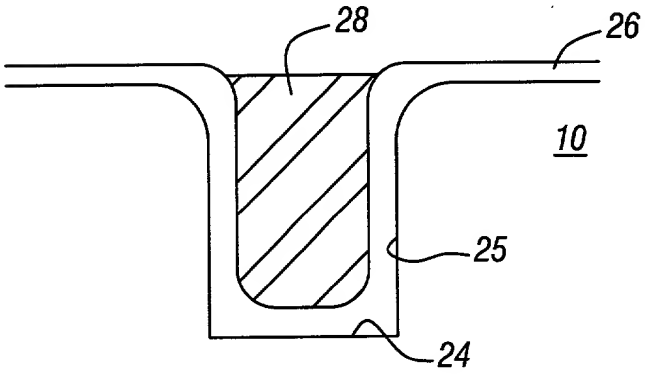

FIG. 6

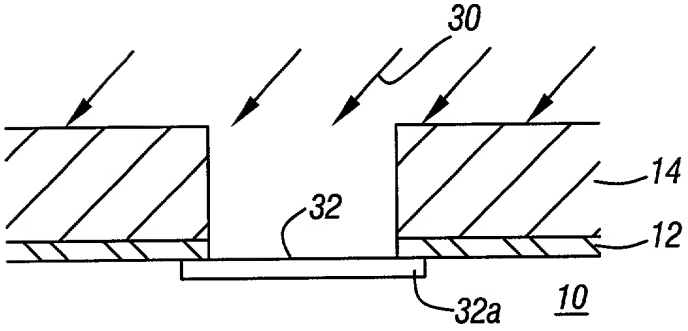

FIG. 7

Attorney Docket No. MICT-0042-US

DECLARATION

SOLE/JOINT INVENTOR
ORIGINAL/SUBSTITUTE/CIP

As a below named inventor, I hereby declare that: my residence, post office address, and citizenship are as stated below next to my name. I believe I am the original, first, and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

FORMING SIDEWALL OXIDE LAYERS FOR TRENCH ISOLATION

as described in the specification ☒ attached or ☐ of patent Application Serial No. _____, filed _____ and amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above; that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application; that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representative or assigns more than twelve months prior to this application; and that I acknowledge the duty to disclose information of which I am aware which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations § 1.56(a). Such information is material when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or
(2) it refutes, or is inconsistent with, a position the applicant has taken or may take in:
(i) opposing an argument of unpatentability relied on by the Office, or
(ii) asserting an argument of patentability.

I hereby claim foreign priority benefits under Title 35, United States Code § 119 of any foreign application(s) for patent or inventor's certificates listed below and have also identified below any foreign application(s) having a filing date before that of the application(s) on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE OF FILING	PRIORITY CLAIMED UNDER 35 USC 119
			☐ YES ☐ NO

I hereby claim the benefit under Title 35 United States Code § 120 of any United States application(s) listed below and, insofar as any subject matter of any claim of this application is not disclosed in the prior United States Application, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations § 1.56(a) which occurred between the filing date of the prior application and the national PCT international filing date of this application:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF SOLE OR FIRST INVENTOR	INVENTOR'S SIGNATURE	DATE:
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant/Patentee: CHANDRA V. MOULI §

Filed: § *Atty File:* MICT-0042-US

Serial No.: §

For: FORMING SIDEWALL OXIDE LAYERS FOR TRENCH ISOLATION §

POWER OF ATTORNEY BY ASSIGNEE

Under the provisions of 37 C.F.R. § 3.71, the undersigned assignee of record of the entire interest in the above-identified patent/patent application by virtue of an assignment recorded (check as applicable):

☒ Concurrently Herewith
☐ Date Recorded _____
☐ Reel _____ Frame _____

elects to conduct the prosecution of the application/maintenance of the patent to the exclusion of the inventor(s). The undersigned hereby declares that he has reviewed the above-referenced assignment and hereby declares that, to the best of his knowledge, title is in the Assignee, and further declares that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true. The assignee hereby revokes any previous powers of attorney and appoints the following to prosecute this application/maintain this patent and transact all business in the Patent and Trademark Office connected therewith:

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The undersigned is authorized to sign this statement on behalf of the Assignee.

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